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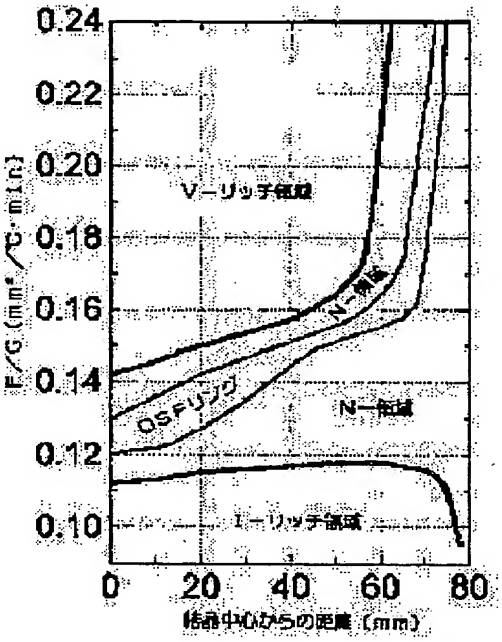
(54) SILICON SINGLE CRYSTAL WAFER WITH LOW CONTENT OF CRYSTAL DEFECT AND ITS PRODUCTION

(57)Abstract:
PROBLEM TO BE SOLVED: To produce a silicon single crystal wafer having a wide control width and an ultralow defect density over the whole surface of the crystal in the absence of both a V-rich region and an I-rich region under readily controllable production conditions by specifying the pulling up conditions of the crystal when growing the silicon single crystal according to a Czochralski (CZ) process.
SOLUTION: A crystal is pulled up in a region surrounded by a border line between a V-rich region and an N-region and a border line between the N-region and an I-rich region in a defect distribution chart indicating the defect distribution for the distance D (mm) from the crystal center to the periphery of the crystal as the abscissa axis versus a value of F/G (mm2/° C.min) as the ordinate axis when the pulling up speed is F (mm/min) and the average value of the gradient of the temperature in the crystal in the pulling up axis direction in a region of temperatures from the melting point of the silicon to 1,400° C is expressed as G (° C/mm). The value of F/G is preferably regulated to 0.112-0.142 mm2/° C.min at the crystal center to pull up the crystal.



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(54)【発明の名称】　結晶欠陥の少ないシリコン単結晶ウエーハ及びその製造方法

(57)【要約】　（修正有）

【課題】　CZ法において制御幅が広く、より制御し易い成長条件下で製造した、熱酸化処理時にOSFリグは発生するが、該リング内外のＮ領域を最大限拡大した低欠陥密度であるシリコン単結晶ウエーハ並びにOSF核は存在するが、熱酸化処理時に該リングは発生せず、かつ、ウエーハ全面の酸素濃度が24ppma以下で、FPD及びL/Dがウエーハ全面内に存在しない、結晶全面が利用可能な極低欠陥密度であるシリコン単結晶ウエーハを提供する。

【解決手段】　CZ法において引上速度をＦ［mm/min］とし、シリコンの融点から1400℃間の引上軸方向の結晶内温度勾配平均値をＧ［℃／mm］で表した時、F/Gの値を結晶中心で0.112 ～0.142mm²／℃･minとする製法、並びに前記F/G 値範囲に制御しかつ結晶中酸素濃度を24ppma以下に抑えて引上げるかまたは結晶中の1050～ 850℃の温度域通過時間を 140分以下に制御する。

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【特許請求の範囲】

【請求項１】　チョクラルスキー法により育成されたシリコン単結晶ウエーハにおいて、熱酸化処理をした際にリング状に発生するＯＳＦリングあるいはＯＳＦリングの核が存在し、かつ、ＦＰＤ及びＬ／Ｄがウエーハ全面内に存在しないことを特徴とするシリコン単結晶ウエーハ。

【請求項２】　チョクラルスキー法により育成されたシリコン単結晶ウエーハにおいて、ウエーハ全面の酸素濃度が２４ｐｐｍａ未満であり、酸素析出熱処理によりＯＳＦリングの潜在核は存在するが、ＯＳＦ熱酸化処理をした際にはＯＳＦリングは発生せず、かつ、ＦＰＤ及びＬ／Ｄがウエーハ全面内に存在しないことを特徴とするシリコン単結晶ウエーハ。

【請求項３】　チョクラルスキー法によってシリコン単結晶を育成する際に、引上げ速度をＦ［ｍｍ／ｍｉｎ］とし、シリコンの融点から１４００℃の間の引上げ軸方向の結晶内温度勾配の平均値をＧ［℃／ｍｍ］で表した時、結晶中心から結晶周辺までの距離Ｄ［ｍｍ］を横軸とし、Ｆ／Ｇ［mm^2／℃・ｍｉｎ］の値を縦軸として欠陥分布を示した欠陥分布図において、Ｖ－リッチ領域とＮ－領域の境界線ならびにＮ－領域とＩ－リッチ領域の境界線で囲繞された領域内で結晶を引上げることを特徴とする、シリコン単結晶ウエーハの製造方法。

【請求項４】　前記Ｆ／Ｇの値を結晶中心で、０．１１２～０．１４２mm^2／℃・ｍｉｎとして結晶を引上げることを特徴とする、請求項３に記載したシリコン単結晶ウエーハの製造方法。

【請求項５】　前記結晶中の１０５０℃から８５０℃までの温度域を通過する時間が１４０分以下となるように制御することを特徴とする、請求項３または請求項４に記載したシリコン単結晶ウエーハの製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、結晶欠陥が少ないシリコン単結晶ウエーハ及びその製造方法に関するものである。

【０００２】

【従来の技術】近年は、半導体回路の高集積化に伴う素子の微細化に伴い、その基板となるチョクラルスキー法（以下、ＣＺ法と略記する）で作製されたシリコン単結晶に対する品質要求が高まってきている。特に、ＦＰＤ、ＬＳＴＤ、ＣＯＰ等のグローンイン（Ｇｒｏｗｎ－ｉｎ）欠陥と呼ばれる酸化膜耐圧特性やデバイスの特性を悪化させる、単結晶成長起因の欠陥が存在しその密度とサイズの低減が重要視されている。

【０００３】これらの欠陥を説明するに当たって、先ず、シリコン単結晶に取り込まれるベイカンシイ（Ｖａｃａｎｃｙ、以下Ｖと略記することがある）と呼ばれる空孔型の点欠陥と、インタースティシアルーシリコン

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（Ｉｎｔｅｒｓｔｉｔｉａｌ－Ｓｉ、以下Ｉと略記することがある）と呼ばれる格子間型シリコン点欠陥のそれぞれの取り込まれる濃度を決定する因子について、一般的に知られていることを説明する。

【０００４】シリコン単結晶において、Ｖ領域とは、Ｖａｃａｎｃｙ、つまりシリコン原子の不足から発生する凹部、穴のようなものが多い領域であり、Ｉ領域とは、シリコン原子が余分に存在することにより発生する転位や余分なシリコン原子の塊が多い領域のことであり、そしてＶ領域とＩ領域の間には、原子の不足や余分が無い（少ない）ニュートラル（Ｎｅｕｔｒａｌ、以下Ｎと略記することがある）領域が存在していることになる。そして、前記グローンイン欠陥（ＦＰＤ、ＬＳＴＤ、ＣＯＰ等）というのは、あくまでもＶやＩが過飽和な状態の時に発生するものであり、多少の原子の偏りがあっても、飽和以下であれば、欠陥としては存在しないことが判ってきた。

【０００５】この両点欠陥の濃度は、ＣＺ法における結晶の引上げ速度（成長速度）と結晶中の固液界面近傍の温度勾配Ｇとの関係から決まり、Ｖ領域とＩ領域との境界近辺にはＯＳＦ（酸化誘起積層欠陥、Ｏｘｉｄａｔｉｏｎ Ｉｎｄｕｓｅｄ Ｓｔａｃｋｉｎｇ Ｆａｕｌｔ）と呼ばれるリング状の欠陥の存在が確認されている。

【０００６】これら結晶成長起因の欠陥を分類すると、成長速度が０．６ｍｍ／ｍｉｎ前後以上と比較的高速の場合には、空孔タイプの点欠陥が集合したボイド起因とされているＦＰＤ、ＬＳＴＤ、ＣＯＰ等のグローンイン欠陥が結晶径方向全域に高密度に存在し、これら欠陥が存在する領域はＶ－リッチ領域と呼ばれている（図４（ａ）参照）。　また、成長速度が０．６ｍｍ／ｍｉｎ以下の場合は、成長速度の低下に伴い、上記したＯＳＦリングが結晶の周辺から発生し、このリングの外側に転位ループ起因と考えられているＬ／Ｄ（Ｌａｒｇｅ Ｄｉｓｌｏｃａｔｉｏｎ：格子間転位ループの略号、ＬＳＥＰＤ、ＬＦＰＤ等）の欠陥が低密度に存在し、これら欠陥が存在する領域はＩ－リッチ領域と呼ばれている（図４（ｂ）参照）。さらに、成長速度を０．４ｍｍ／ｍｉｎ前後と低速にすると、ＯＳＦリングがウエーハの中心に凝集して消滅し、全面がＩ－リッチ領域となる（図４（ｃ））。

【０００７】また、最近Ｖ－リッチ領域とＩ－リッチ領域の中間でＯＳＦリングの外側に、Ｎ領域と呼ばれる、空孔起因のＦＰＤ、ＬＳＴＤ、ＣＯＰも、転位ループ起因のＬＳＥＰＤ、ＬＦＰＤも存在しない領域の存在が発見されている（特開平８－３３０３１６号参照）。この領域はＯＳＦリングの外側にあり、そして、酸素析出熱処理を施し、Ｘ－ｒａｙ観察等で析出のコントラストを確認した場合に、酸素析出がほとんどなく、かつ、ＬＳＥＰＤ、ＬＦＰＤが形成されるほどリッチではないＩ－

リッチ領域側であると報告している（図３（ａ）参照）。そして、従来のＣＺ引上げ機ではウエーハの極一部にしか存在しないＮ領域を、引上げ機の炉内温度分布を改良し、引上げ速度を調節して、Ｆ／Ｇ値（単結晶引上げ速度をＦ［ｍｍ／ｍｉｎ］とし、シリコンの融点から１３００℃の間の引上げ軸方向の結晶内温度勾配の平均値をＧ［℃／ｍｍ］とするとき、Ｆ／Ｇで表わされる比）を０．２０～０．２２ｍｍ²／℃・ｍｉｎとしてウエーハ全面及び結晶全長に対して制御すれば、Ｎ領域をウエーハ全面に広げることが可能であると提案している（図３（ｂ）参照）。

【０００８】

【発明が解決しようとする課題】しかしながら、このような極低欠陥領域を結晶全体に広げて製造しようとすると、この領域がＩ－リッチ領域側のＮ領域のみに限定されるため、製造条件の上で制御範囲が極めて狭く、実験機ならともかく生産機では精密制御が難しく、生産性に難点があって実用的でない。さらに、この発明に開示されていた欠陥分布図は、本発明者らが実験・調査して求めたデータや、データを基にした作成した欠陥分布図（図１参照）とは大幅に異なることが判明した。

【０００９】本発明は、このような問題点に鑑みなされたもので、制御幅が広く、制御し易い製造条件の下で、Ｖ－リッチ領域およびＩ－リッチ領域のいずれも存在しない、結晶全面に亙って極低欠陥密度であるＣＺ法によるシリコン単結晶ウエーハを、高生産性を維持しながら得ることを目的とする。

【００１０】

【課題を解決するための手段】本発明は、前記目的を達成するために為されたもので、本発明の請求項１に記載した発明は、ＣＺ法により育成されたシリコン単結晶ウエーハにおいて、熱酸化処理をした際にリング状に発生するＯＳＦリングあるいはＯＳＦリングの核が存在し、かつ、ＦＰＤ及びＬ／Ｄがウエーハ全面内に存在しないことを特徴とするシリコン単結晶ウエーハである。

【００１１】そして、このようなシリコン単結晶ウエーハの製造方法としては、本発明の請求項３に記載したように、チョクラルスキー法によってシリコン単結晶を育成する際に、引上げ速度をＦ［ｍｍ／ｍｉｎ］とし、シリコンの融点から１４００℃の間の引上げ軸方向の結晶内温度勾配の平均値をＧ［℃／ｍｍ］で表した時、結晶中心から結晶周辺までの距離Ｄ［ｍｍ］を横軸とし、Ｆ／Ｇ［ｍｍ²／℃・ｍｉｎ］の値を縦軸として欠陥分布を示した欠陥分布図において、Ｖ－リッチ領域とＮ－領域の境界線ならびにＮ－領域とＩ－リッチ領域の境界線で囲繞された領域内で結晶を引上げることを特徴とする、シリコン単結晶ウエーハの製造方法である。

【００１２】このように、実験・調査の結果を解析して求めた図１の欠陥分布図を基に、Ｖ－リッチ領域とＮ－領域の境界線ならびにＮ－領域とＩ－リッチ領域の境界

線で囲繞された領域内に収まるように、結晶の引上げ速度Ｆとシリコンの融点から１４００℃の間の引上げ軸方向の結晶内温度勾配の平均値Ｇを制御して結晶を引上げれば、前記請求項１に記載した、熱酸化処理をした際にリング状に発生するＯＳＦリングあるいはＯＳＦリングの核が存在し、かつ、ＦＰＤ及びＬ／Ｄがウエーハ全面内に存在しないシリコン単結晶ウエーハを作製することができる。

【００１３】さらに、具体的には、　前記Ｆ／Ｇの値を結晶中心で、０．１１２～０．１４２ｍｍ²／℃・ｍｉｎとして結晶を引上げることとした（請求項４）。

【００１４】このように、Ｆ／Ｇの値を結晶中心で、０．１１２～０．１４２ｍｍ²／℃・ｍｉｎに制御することによって、図１に見られるように、熱酸化処理時にＯＳＦリングを発生し得る領域を含んだままではあるが、ＯＳＦリング内外のＮ領域を最大限拡大するようにして引上げるので、引上げ速度と結晶内温度勾配との制御範囲が広くなり生産機においても製造条件設定が容易になり、Ｎ領域の多いウエーハを簡単に作製することができる。

【００１５】このように、本発明の請求項３または請求項４に記載の製造方法によって得られたシリコン単結晶ウエーハは、該ウエーハを熱酸化処理をした際に、リング状にＯＳＦリングは発生し、あるいはＯＳＦリングの核は潜在しているが、ＦＰＤ及びＬ／Ｄ（ＬＳＥＰＤ、ＬＦＰＤ）は、ウエーハ全面内に存在しないというウエーハで、図２（ｂ）に示したように、いわゆるウエーハ全面にＶ－リッチ領域とＩ－リッチ領域は存在せず、中性なＮ領域の面積が非常に大きなものである。このようなＮ領域の大きい本発明のシリコンウエーハには、ＯＳＦリングの核は潜在しており、該ウエーハを熱酸化処理した際にはリング状にＯＳＦが発生し得るＯＳＦリングの内側にもＮ領域が存在することを利用して、前記ＯＳＦリング外側のＮ領域とＯＳＦリング内側のＮ領域を最大限に拡大した新規な欠陥構造を持ったウエーハである。

【００１６】そして、本発明の請求項２に記載した発明は、ＣＺ法により育成されたシリコン単結晶ウエーハにおいて、ウエーハ全面の酸素濃度が２４ｐｐｍａ（ＡＳＴＭ’７９値）未満であり、酸素析出熱処理によりＯＳＦリングの潜在核は存在するが、ＯＳＦ熱酸化処理をした際にはＯＳＦリングは発生せず、かつ、ＦＰＤ及びＬ／Ｄがウエーハ全面内に存在しないことを特徴とするシリコン単結晶ウエーハである。そして、このようなシリコン単結晶ウエーハの製造方法としては、本発明の請求項５に記載したように、請求項３または請求項４に記載した製造方法に加えて、前記結晶中の１０５０℃から８５０℃までの温度域を通過する時間が１４０分以下となるように制御するようにした。

【００１７】このように、成長結晶内の酸素濃度を２４

ppma未満に抑え、あるいは成長結晶中の1050℃から850℃までの温度域を通過する時間を140分以下となるように熱履歴を制御すれば、OSF核の成長を阻害することができ、実質上、OSFリングあるいはOSFリングの潜在核がウエーハ内に存在してもデバイスに影響を与えることはないので、結局該ウエーハをOSF熱酸化処理をした際に、OSFリングの核は潜在しているが、OSFリングを発生することはなく、FPD及びL／D（LSEPD、LFPD）もウエーハ全面内に存在しないという、いわゆるウエーハ全面がV－リッチ領域、I－リッチ領域も、害を及ぼすようなOSFリングも存在しない全面使用可能な結晶全面に亙って極低欠陥密度なウエーハを得ることができる。しかもこの場合、F／Gの制御も広い制御範囲とすることが可能であり、ウエーハを実用上容易に作製することができる。

【0018】以下、本発明につき詳細に説明するが、本発明はこれらに限定されるものではない。説明に先立ち各用語につき予め解説しておく。

1）FPD（Flow Pattern Defect）とは、成長後のシリコン単結晶棒からウェーハを切り出し、表面の歪み層を弗酸と硝酸の混合液でエッチングして取り除いた後、$K_2Cr_2O_7$と弗酸と水の混合液で表面をエッチング（Seccoエッチング）することによりピットおよびさざ波模様が生じる。このさざ波模様をFPDと称し、ウェーハ面内のFPD密度が高いほど酸化膜耐圧の不良が増える（特開平4－192345号公報参照）。

【0019】2）SEPD（Secco Etch Pit Defect）とは、FPDと同一のSeccoエッチングを施した時に、流れ模様（flow pattern）を伴うものをFPDと呼び、流れ模様を伴わないものをSEPDと呼ぶ。この中で10μm以上の大きいSEPD（LSEPD）は転位クラスターに起因すると考えられ、デバイスに転位クラスターが存在する場合、この転位を通じて電流がリークし、P－Nジャンクションとしての機能を果たさなくなる。

【0020】3）LSTD（Laser Scattering Tomography Defect）とは、成長後のシリコン単結晶棒からウエーハを切り出し、表面の歪み層を弗酸と硝酸の混合液でエッチングして取り除いた後、ウエーハを劈開する。この劈開面より赤外光を入射し、ウエーハ表面から出た光を検出することでウエーハ内に存在する欠陥による散乱光を検出することができる。ここで観察される散乱体については学会等ですでに報告があり、酸素析出物とみなされている（J．J．A．P．　Vol．32，P3679，1993参照）。また、最近の研究では、八面体のボイド（穴）であるという結果も報告されている。

【0021】4）COP（Crystal Originated Particle）とは、ウエーハの中心部の酸化膜耐圧を劣化させる原因となる欠陥で、Seccoエッチ ではFPDになる欠陥が、SC－1洗浄（$NH_4OH:H_2O_2:H_2O=1:1:10$の混合液による洗浄）では選択エッチング液として働き、COPになる。このピットの直径は1μm以下で光散乱法で調べる。

【0022】5）L／D（Large Dislocation：格子間転位ループの略号）には、LSEPD、LFPD等があり、転位ループ起因と考えられている欠陥である。LSEPDは、上記したようにSEPDの中でも10μm以上の大きいものをいう。また、LFPDは、上記したFPDの中でも先端ピットの大きさが10μm以上の大きいものをいい、こちらも転位ループ起因と考えられている。

【0023】本発明者らは、先に特願平9－199415号で提案したように、CZ法によるシリコン単結晶成長に関し、V領域とI領域の境界近辺について、詳細に調査したところ、この境界近辺の極く狭い領域にFPD、LSTD、COPの数が著しく少なく、LSEPDも存在しないニュートラルな領域があることを発見した。

【0024】そこで、このニュートラルな領域をウエーハ全面に広げることができれば、点欠陥を大幅に減らせると発想し、成長（引上げ）速度と温度勾配の関係の中で、結晶のウエーハ面内では、引上げ速度はほぼ一定であるから、面内の点欠陥の濃度分布を決定する主な因子は温度勾配である。つまり、ウエーハ面内で、軸方向の温度勾配に差があることが問題で、この差を減らすことが出来れば、ウエーハ面内の点欠陥の濃度差も減らせることを見出し、結晶中心部の温度勾配Gcと結晶周辺部分の温度勾配Geとの差を$\triangle G=(Ge-Gc)\leqq 5$℃／cmとなるように炉内温度を制御して引上げ速度を調節すれば、ウエーハ全面がN領域からなる欠陥のないウエーハが得られるようになった。

【0025】本発明では、上記のような温度勾配の差△Gが小さいCZ法による結晶引上げ装置を使用し、引上げ速度を変えて結晶面内を調査した結果、新たに次のような知見を得た。V－リッチ領域とI－リッチ領域の間に存在するN領域は、従来はOSFリング（核）の外側のみと考えられていたが、OSFリングの内側にも、N領域が存在することを確認した（図2（a）参照）。すなわち、上記特願平9－199415号の場合、OSFリングは、V－リッチ領域とN領域の境界領域となっていた（図3（a）参照）が、この二つは必ずしも一致しないことがわかった。このことは従来の△Gの大きい結晶引上げ装置で実験した場合には発見されず、今回上記の△Gの小さい結晶引上げ装置を使用した結晶を調査した結果、発見したものである。

【0026】この調査における引上げ装置の炉内温度を、総合伝熱解析ソフトFEMAG（F．Dupre

t, P. Nicodeme, Y. Ryckmans, P. Wouters, and M. J. Crochet, Int. J. Heat MassTransfer, 33, 1849（1990））を使用して鋭意解析を行った。その結果、引上げ速度をF［mm／min］とし、シリコンの融点から１４００℃の間の引上げ軸方向の結晶内温度勾配の平均値をG［℃／mm］で表した時、F／Gの値を結晶中心で、０．１１２～０．１４２mm² ／℃・minの範囲内となるように引上げ速度Fと温度勾配平均値Gとを制御すれば、ＯＳＦ熱酸化処理をした際にリング状に発生するＯＳＦリングあるいはＯＳＦリングの核が存在するものの、ＦＰＤ及びＬ／Ｄがウエーハ全面内に存在しないシリコン単結晶ウエーハが得られることが判った。

【００２７】図１は、直径６インチのシリコン単結晶を例とした場合であるが、結晶の径方向位置を横軸とし、Ｆ／Ｇ値を縦軸とした場合の諸欠陥分布を表している。図１から明らかなように、Ｖ－リッチ領域／Ｎ領域の境界は、結晶中心位置と中心から約５０mmまでの位置との間では０．１４２mm² ／℃・minから緩やかに上昇し、この位置から外周にかけては急激にＦ／Ｇ値を増大した線上にある。ＯＳＦリング領域の中心は、約０．１２５mm² ／℃・minで、結晶外周にかけてはＶ－リッチ領域／Ｎ領域の境界線とほぼ平行して急激にＦ／Ｇ値を増大した線上にある。さらにＮ領域／Ｉ－リッチ領域との境界は、結晶中心位置と中心から約７０mmまでの位置との間で０．１１２mm² ／℃・minとなり、その後、結晶外周に向って急激に落ち込んでいる。従って、ＯＳＦリングを含むそのウエーハ内のＮ領域を最大限に利用するには、結晶中心位置で０．１１２～０．１４２mm² ／℃・minとなるようにすればよい。

【００２８】これをウエーハの面で説明すると、従来は、図３（ａ）に示したように、通常の引上げ速度と結晶引上げ装置におけるＯＳＦリングの外側に存在するＮ領域を結晶全面に拡大すべく（図３（ｂ）参照）、特別な結晶引上げ装置を用いて引上げ速度と△Ｇを制御し、無欠陥結晶を製造しようとしていたが、引上げ速度、温度勾配等製造条件の制御幅が極めて狭く、制御が困難で生産性に難点があり、実用的でなかった。

【００２９】本発明では、ＯＳＦリングの外側のＮ領域だけに限定せず、今回発見したＯＳＦリングの内側にも存在するＮ領域（図２（ａ）参照）をも使用してＮ領域を最大限拡大することにした。すなわち、図２（ｂ）に示したようにＯＳＦリングを含んだままＮ領域を最大限ウエーハ全面に拡大することができる引上げ速度と△Ｇ及び結晶引上げ装置を選択して引上げた。その結果、上記したようなＦ／Ｇ値の範囲内に収まるように引上げ速度と結晶内温度勾配を調整して引上げれば、従来よりも拡大された制御幅をもつ製造条件下で容易に低欠陥のウエーハを製造することができる。

【００３０】一方、ＯＳＦリングについては、最近の研究からウエーハ全面内で低酸素濃度の場合には、ＯＳＦリングの核が存在しても熱酸化処理によりＯＳＦリングを発生することはなく、デバイスに影響を与えないということが判ってきている。この酸素濃度の限界値は、同一の結晶引上げ装置を使用して、数種類の酸素濃度レベルの結晶を引上げた結果、ウエーハ全面内の酸素濃度が２４ｐｐｍａ未満であれば、ウエーハの熱酸化処理を行った時にＯＳＦリングが発生しないことが確認されている。

【００３１】すなわち、図５は、一本の結晶を引上げ中に徐々に酸素濃度を下げていった時に、結晶全長にわたってＯＳＦとなる核は存在するが、ウエーハの熱酸化処理を行った時にＯＳＦリングが観察されるのは２４ｐｐｍａまでで、２４ｐｐｍａ未満ではＯＳＦリング核は存在するが、熱酸化処理によるＯＳＦリングは発生していないことを表している。

【００３２】ちなみに、成長結晶中の酸素濃度を２４ｐｐｍａ未満にするには、従来から一般に用いられている方法で行えばよく、例えば、ルツボの回転数あるいは融液内温度分布等を調整して融液の対流を制御する等の手段により簡単に行うことができる。

【００３３】なお、ＯＳＦリングは発生しなくても、その核の存在するところでは酸素析出が少なくなるという傾向があるが、デバイスの低温下プロセスにおいては、強いゲッタリングも要求されないので、ＯＳＦ領域での酸素析出の少なさは問題にならない。

【００３４】次いでＯＳＦリング核の成長を阻害する条件を検討した。炉内温度分布の異なる結晶引上げ装置（炉内構成を変更したもの）を数種類使用して、ＯＳＦ熱酸化処理時にＯＳＦリングが発生するように、引上げ速度を制御して結晶を引上げた結果、１０５０～８５０℃の温度帯域を１４０分以下で通過する熱履歴を与えた結晶には、その後ＯＳＦリング発生の有無を確認するＯＳＦ熱酸化処理を施してもＯＳＦリングは確認されなかった（I. Yamashita and Y. Shimanuki：The Electrochemical SocietyExtended Abstract, Los Angels, Carifornia, May7－12, 1989, P. 346参照）。

【００３５】そこで、Ｆ／Ｇ値制御に加えて、結晶中酸素濃度を２４ｐｐｍａ未満に抑え、あるいは、成長結晶の１０５０℃から８５０℃までの温度域を通過する熱履歴を１４０分以下となるように制御してＯＳＦリング核の成長を阻害すれば、ＯＳＦ熱酸化処理をした際にはＯＳＦリングの発生はなく、かつ、ＦＰＤ及びＬ／Ｄが存在せず、結晶全面が使用可能な領域で占められ、無欠陥の結晶を広い条件範囲で作製することができる。

【００３６】すなわち、ＣＺ法によってシリコン単結晶

を育成する際に、引上げ速度をＦ［ｍｍ／ｍｉｎ］とし、シリコンの融点から１４００℃の間の引上げ軸方向の結晶内温度勾配の平均値をＧ［℃／ｍｍ］で表した時、Ｆ／Ｇの値を結晶中心で、０．１１２～０．１４２ｍｍ²／℃・ｍｉｎに制御し、結晶中酸素濃度を２４ｐｐｍａ未満に抑え、あるいは、前記結晶中の１０５０℃から８５０℃までの温度域を通過する時間が１４０分以下となるように制御することによって、広いＮ領域を持つと共に熱酸化処理をしてもＯＳＦリングが発生しない、全面使用可能な無欠陥ウエーハを制御幅の広い条件下で容易に製造することができる。

【００３７】

【発明の実施の形態】以下、本発明の実施の形態について、図面を参照しながら詳細に説明する。まず、本発明で使用するＣＺ法による単結晶引上げ装置の構成例を図６により説明する。図６に示すように、この単結晶引上げ装置３０は、引上げ室３１と、引上げ室３１中に設けられたルツボ３２と、ルツボ３２の周囲に配置されたヒータ３４と、ルツボ３２を回転させるルツボ保持軸３３及びその回転機構（図示せず）と、シリコンの種子結晶５を保持するシードチャック６と、シードチャック６を引上げるケーブル７と、ケーブル７を回転又は巻き取る巻取機構（図示せず）を備えて構成されている。ルツボ３２は、その内側のシリコン融液（湯）２を収容する側には石英ルツボが設けられ、その外側には黒鉛ルツボが設けられている。また、ヒータ３４の外側周囲には断熱材３５が配置されている。

【００３８】また、本発明の製造方法に関わる製造条件を設定するために、結晶の固液界面の外周に環状の固液界面断熱材８を設け、その上に上部囲繞断熱材９が配置されている。この固液界面断熱材８は、その下端とシリコン融液２の湯面との間に３～５ｃｍの隙間１０を設けて設置されている。上部囲繞断熱材９は条件によっては使用しないこともある。さらに、冷却ガスを吹き付けたり、輻射熱を遮って単結晶を冷却する筒状の冷却装置３６を設けている。別に、最近では引上げ室３１の水平方向の外側に、図示しない磁石を設置し、シリコン融液２に水平方向あるいは垂直方向等の磁場を印加することによって、融液の対流を抑制し、単結晶の安定成長をはかる、いわゆるＭＣＺ法が用いられることも多い。

【００３９】次に、上記の単結晶引上げ装置３０による単結晶育成方法について説明する。まず、ルツボ３２内でシリコンの高純度多結晶原料を融点（約１４２０°Ｃ）以上に加熱して融解する。次に、ケーブル７を巻き出すことにより融液２の表面略中心部に種子結晶５の先端を接触又は浸漬させる。その後、ルツボ保持軸３３を適宜の方向に回転させるとともに、ケーブル７を回転させながら巻き取り種子結晶５を引上げることにより、単結晶育成が開始される。以後、引上げ速度と温度を適切に調節することにより略円柱形状の単結晶棒１を得ることができる。

【００４０】この場合、本発明では、本発明の目的を達成するために特に重要であるのは、図６に示したように、引上げ室３１の湯面上の単結晶棒１中の液状部分の外周空間において、湯面近傍の結晶の温度が１４２０℃から１４００℃までの温度域に環状の固液界面断熱材８を設けたことと、その上に上部囲繞断熱材９を配置したことである。さらに、必要に応じてこの断熱材の上部に結晶を冷却する装置、例えば冷却装置３６を設けて、これに上部より冷却ガスを吹きつけて結晶を冷却できるものとし、筒下部に輻射熱反射板を取り付けた構造としてもよい。

【００４１】このように液面の直上の位置に所定の隙間を設けて断熱材を配置し、さらにこの断熱材の上部に結晶を冷却する装置を設けた構造とすることによって、結晶成長界面近傍では輻射熱により保温効果が得られ、結晶の上部ではヒータ等からの輻射熱をカットできるので、本発明の製造条件を満足させることができる。この結晶の冷却装置としては、前記筒状の冷却装置３６とは別に、結晶の周囲を囲繞する空冷ダクトや水冷蛇管等を設けて所望の温度勾配を確保するようにしても良い。

【００４２】本発明で使用した単結晶引上げ装置と比較のために従来の装置を図７に示した。　基本的な構造については、本発明で使用した引上げ装置と同じであるが、固液界面断熱材８、上部囲繞断熱材９や冷却装置３６は装備していない。

【００４３】

【実施例】以下、本発明の具体的な実施の形態を実施例を挙げて説明するが、本発明はこれらに限定されるものではない。

（実施例１）図６に示した引上げ装置３０で、２０インチ石英ルツボに原料多結晶シリコンを６０Ｋｇチャージし、直径６インチ、方位＜１００＞のシリコン単結晶棒を平均引上げ速度を０．８８～０．５０ｍｍ／ｍｉｎに下げながら引上げを行った（単結晶棒の直胴長さ約８５ｃｍ）。シリコン融液の湯温は約１４２０℃、湯面から環状の固液界面断熱材の下端までは、４ｃｍの空間とし、その上に１０ｃｍ高さの環状固液界面断熱材を配置し、湯面から引上げ室天井までの高さをルツボ保持軸を調整して３０ｃｍに設定し、上部囲繞断熱材を配備した。そして、結晶中心部でのＦ／Ｇ値を０．２２～０．１０ｍｍ²・℃／ｍｉｎに変化させて引上げた。

【００４４】ここで得られた単結晶棒から、ウエーハを切り出し、鏡面加工を施してシリコン単結晶の鏡面ウエーハを作製し、グローンイン欠陥の測定を行った。また、熱酸化処理を施してＯＳＦリング発生の有無を確認した。その結果、Ｆ／Ｇ値が０．１１２～０．１４２ｍｍ²／℃・ｍｉｎの範囲内において、ウエーハ外周部より約１５ｍｍ位置に熱酸化処理時に発生するＯＳＦリング領域は存在するが、該リング内外のグローンイン欠陥

の存在しないＮ領域を最大限拡大した極低欠陥ウエーハを得た。なお、このウエーハの酸化膜耐圧特性は、Ｃ－モード良品率１００％となった。なお、Ｃ－モード測定条件は、次の通りである。

１）酸化膜厚：２５ｎｍ、　２）測定電極：リンドープ・ポリシリコン、

３）電極面積：８ｍｍ²、　４）判定電流：１ｍＡ／ｃｍ²、

５）良品判定：絶縁破壊電界が８ＭＶ／ｃｍ以上のものを良品と判定した。

【００４５】（実施例２）単結晶引上げ中に徐々に酸素濃度を下げて行った以外は実施例１と同一条件で引上げ、得られた単結晶棒から、ウエーハを切り出し、鏡面加工を施してシリコン単結晶の鏡面ウエーハを作製し、グローンイン欠陥の測定を行った。また、熱酸化処理を施してＯＳＦリング発生の有無を確認した。

【００４６】その結果、Ｆ／Ｇ値が０．１１２～０．１４２ｍｍ²／℃・ｍｉｎの範囲内において、ウエーハ面内酸素濃度が２４ｐｐｍａ以上のウエーハは全面グローンイン欠陥の存在しないＮ領域でウエーハ中心から約１５ｍｍ位置にＯＳＦリングを有する極低欠陥ウエーハであった。これに対してウエーハ面内酸素濃度が２４ｐｐｍａ未満のウエーハは全面グローンイン欠陥の存在しないＮ領域で、ＯＳＦ核は存在するが熱酸化処理によってＯＳＦリングを発生しない無欠陥ウエーハであった。なお、このウエーハの酸化膜耐圧特性は、Ｃ－モード良品率１００％となった。

【００４７】（実施例３）単結晶引上げ中に、結晶中の１０５０～８５０℃までの温度域を通過する時間を１４０分以下とした熱履歴を与えた以外は実施例１と同一条件で引上げ、得られた単結晶棒から、ウエーハを切り出し、鏡面加工を施してシリコン単結晶の鏡面ウエーハを作製し、グローンイン欠陥の測定を行った。また、熱酸化処理を施してＯＳＦリング発生の有無を確認した。

【００４８】その結果、酸素濃度が２７ｐｐｍａのものであっても、Ｆ／Ｇ値が０．１１２～０．１４２ｍｍ²／℃・ｍｉｎの範囲内において、全面グローンイン欠陥の存在しないＮ領域で、ＯＳＦ核は存在するが熱酸化処理によってＯＳＦリングを発生しない無欠陥ウエーハであった。なお、このウエーハの酸化膜耐圧特性は、Ｃ－モード良品率１００％となった。

【００４９】なお、本発明は、上記実施形態に限定されるものではない。上記実施形態は、例示であり、本発明の特許請求の範囲に記載された技術的思想と実質的に同一な構成を有し、同様な作用効果を奏するものは、いかなるものであっても本発明の技術的範囲に包含される。

【００５０】例えば、上記実施形態においては、直径６インチのシリコン単結晶を育成する場合につき例を挙げて説明したが、本発明はこれには限定されず、引上げ速度をＦ［ｍｍ／ｍｉｎ］とし、シリコンの融点から１４００℃の間の引上げ軸方向の結晶内温度勾配の平均値をＧ［℃／ｍｍ］で表した時、Ｆ／Ｇの値を結晶中心で、０．１１２～０．１４２ｍｍ²／℃・ｍｉｎとなるように制御すれば、直径８～１６インチあるいはそれ以上のシリコン単結晶にも適用できる。また、本発明は、シリコン融液に水平磁場、縦磁場、カスプ磁場等を印加するいわゆるＭＣＺ法にも適用できることは言うまでもない。

【００５１】さらに、上記実施形態においては、低酸素化と熱履歴制御を別々に説明したが、両者を共に実施してもよく、より確実にＯＳＦリングを無害化することができる。

【００５２】

【発明の効果】以上説明したように、本発明によれば、単結晶育成条件の制御幅が広くなり、ＯＳＦリング外側のＮ領域、ＯＳＦリング、あるいはＯＳＦ核及びその内側のＮ領域も使用することにより最大限Ｎ領域を拡大したウエーハを容易に作製することができる。そして、低酸素化あるいは低温域の熱履歴の制御を併用すればＯＳＦリングも発生せず、グローイン欠陥も極低レベルのウエーハ全面が無欠陥のシリコン単結晶ウエーハを製造することができる。

【図面の簡単な説明】

【図１】シリコン単結晶ウエーハ面内における、結晶の径方向位置を横軸とし、Ｆ／Ｇ値を縦軸とした場合の諸欠陥分布図である。

【図２】本発明で発見した結晶面内諸欠陥分布を表した説明図である。

（ａ）通常の引上げ条件で引上げた場合、（ｂ）本発明の引上げ条件で引上げた場合。

【図３】従来の引上げ方法における結晶面内諸欠陥分布を表した説明図である。

（ａ）通常の引上げ条件で引上げた場合、（ｂ）引上げ速度と結晶内温度勾配を精密制御して引上げた場合。

【図４】従来の引上げ方法における引上げ速度と結晶面内欠陥分布との関係を表した説明図である。

（ａ）高速引上げの場合、（ｂ）中速引上げの場合、

（ｃ）低速引上げの場合。

【図５】本発明において、ウエーハに熱酸化処理を施した際のＯＳＦリングの発生領域とＯＳＦ核の存在領域との境界位置が結晶中酸素濃度に影響されていることを表した説明図である。

（ａ）結晶棒の長さ方向位置と酸素濃度の関係を表したグラフ、（ｂ）結晶縦断面において、ＯＳＦリングの発生領域とＯＳＦ核の存在領域との境界位置を示す説明図である。

【図６】　本発明で使用したＣＺ法による単結晶引上げ装置の概略説明図である。

【図７】ＣＺ法による従来の単結晶引上げ装置の概略説明図である。

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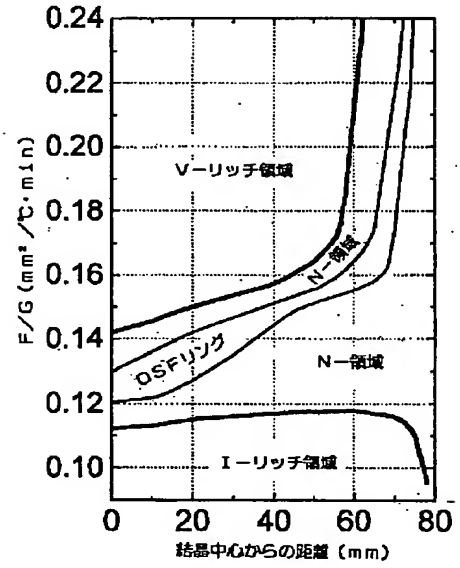
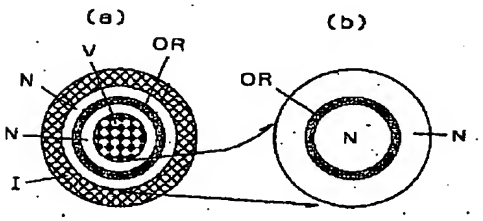
【符号の説明】
1…成長単結晶棒、
2…シリコン融液、
3…湯面、
4…固液界面、
5…種子結晶、
6…シードチャック、
7…ケーブル、
8…固液界面断熱材、
9…上部囲繞断熱材、
１０…湯面と固液界面断熱材下端との隙間、
＊３０…単結晶引上げ装置、
３１…引上げ室、
３２…ルツボ、
３３…ルツボ保持軸、
３４…ヒータ、
３５…断熱材、
３６…冷却装置。
V　…Vーリッチ領域、
N　…Nー領域、
I　…Iーリッチ領域、
＊　OR…OSFリング。

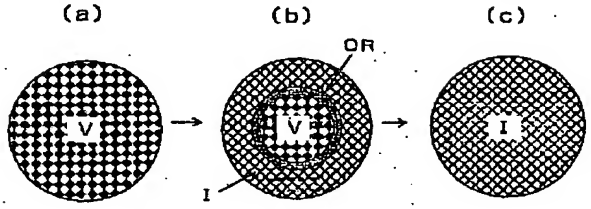
【図１】



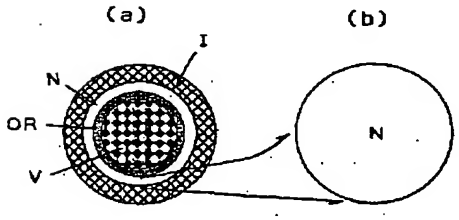
【図２】



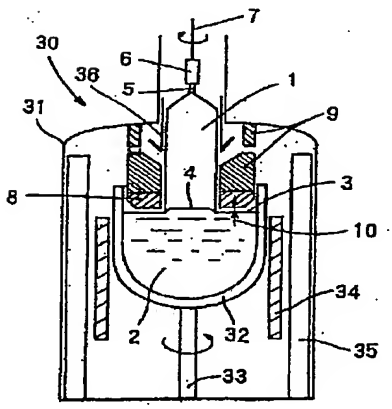
【図４】



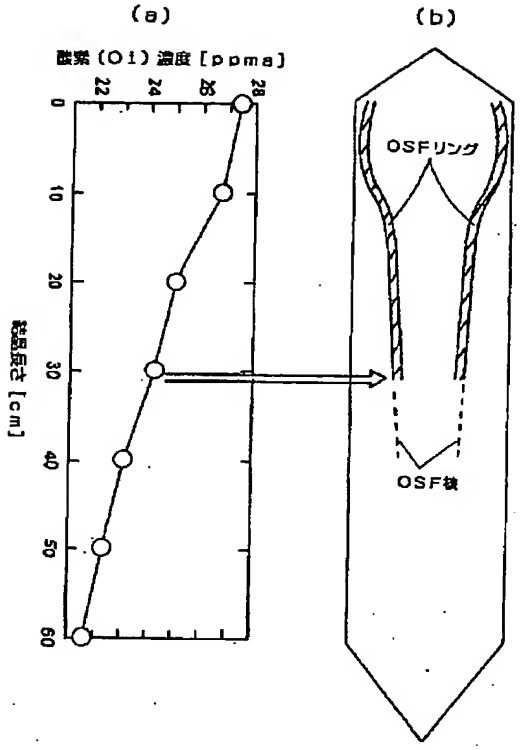
【図３】



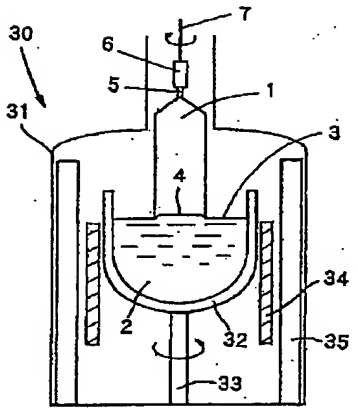
【図６】



【図５】



【図７】



フロントページの続き

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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] The silicon single crystal wafer characterized by for the nucleus of the OSF ring generated in the shape of a ring or an OSF ring existing in the silicon single crystal wafer raised by the Czochrlski method when thermal oxidation processing is carried out, and FPD and ratio of length to diameter not existing in the whole wafer surface.
[Claim 2] It is the silicon single crystal wafer characterized by not generating an OSF ring and FPD and ratio of length to diameter not existing in the whole wafer surface when OSF thermal oxidation processing is carried out although the oxygen density of the whole wafer surface is less than 24 ppmas and the potential nucleus of an OSF ring exists by oxygen precipitation heat treatment in the silicon single crystal wafer raised by the Czochrlski method.
[Claim 3] In case a silicon single crystal is raised with the Czochrlski method, a pull-up rate is set to F [mm/min]. When the average of inclination is expressed with G [**/mm] from the melting point of silicon whenever [crystal internal temperature / of the pull-up shaft orientations between 1400 degrees C], In the defective distribution map in which having set the axis of abscissa as the distance D from a crystal center to the crystal circumference [mm], and having shown defective distribution by setting an axis of ordinate as the value of F/G [mm2 / **, and min] The manufacture approach of the silicon single crystal wafer characterized by pulling up a crystal in the field surrounded by the boundary line of a V-rich field and N-field, and the boundary line of N-field and an I-rich field.
[Claim 4] The manufacture approach of the silicon single crystal wafer indicated to claim 3 characterized by pulling up a crystal for the value of said F/G as 0.112-0.142mm2/degree C and min in a crystal center.
[Claim 5] The manufacture approach of the silicon single crystal wafer indicated to claim 3 or claim 4 characterized by controlling so that the time amount which passes through the temperature region from 1050 degrees C to 850 degrees C under said crystal becomes 140 or less minutes.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to a silicon single crystal wafer with few crystal defects, and its manufacture approach.
[0002]
[Description of the Prior Art] In recent years, the quality demand to the silicon single crystal produced with the Czochrlski method (it is hereafter written as a CZ process) used as the substrate has been increasing with detailed-izing of the component accompanying high integration of a semiconductor circuit. The defect of a single crystal growth reason in which the oxide film proof-pressure property especially called grown-in (Grown-in) defects, such as FPD, LSTD, and COP, and the property of a device are worsened exists, and importance is attached to reduction of the consistency and size.
[0003] In explaining these defects, it explains being known generally about the factor which determines each concentration of the point defect of the hole mold first called the Vacancy (it may outline Vacancy and Following V) incorporated by the silicon single crystal, and the mold silicon point defect between grids called Interstitial-Si (it may outline Interstitial-Si and Following I) incorporated.
[0004] In a silicon single crystal, V fields are Vacancy, i.e., the crevice generated from lack of a silicon atom, and a field with many things like a hole. With an I region It is the thing of a field with many lumps of the rearrangement and the excessive silicon atom which are generated when a silicon atom exists too much. Between V field and an I region The neutral (it may outline Neutral and Following N) field without lack of an atom or an excess (few) will exist. And with [even if said grown-in defects (FPD, LSTD, COP, etc.) occur when V and I are in a condition / ****** / to the last, and it has the bias of some atoms] saturation [below], it has turned out that it does not exist as a defect.
[0005] The concentration of both this point defect is decided from the pull-up rate (growth rate) of the crystal in a CZ process, and relation with the temperature gradient G near [under crystal] the solid-liquid interface, and existence of the defect of the shape of a ring called OSF (an oxidation induction stacking fault, Oxidation Indused Stacking Fault) is checked in the boundary neighborhood of V field and an I region.
[0006] A classification of the defect of these crystal growth reason calls the V-rich field the field where grown-in defects by which it is considered as the void reason to which hole type point defects gathered when a growth rate is a high speed comparatively, the above before and after 0.6 mm/min and, such as FPD, LSTD, and COP, exist in high density throughout the direction of the diameter of a crystal, and these defects exist (refer to drawing 4 (a)). Moreover, when a growth rate is 0.6 or less mm/min, the field where the above-mentioned OSF ring is generated from the circumference of a crystal with the fall of a growth rate, the defect of ratios of length to diameter (Large Dislocation: the cable address of the dislocation loop between grids, LSEPD, LFPD, etc.) considered to be dislocation loop reasons by the outside of this ring exists in a low consistency, and these defects exist is called the I-rich field (refer to drawing 4 (b)). Furthermore, if a growth rate is made into a low speed 0.4 mm/min order, an OSF ring will condense and disappear at the core of a wafer, and the whole surface will serve as an I-rich field (drawing 4 (c)).

[0007] Moreover, the existence of the field where neither FPD of a hole reason, LSTD, COP nor LSEPD of a dislocation loop reason and LFPD exist called N field to the outside of an OSF ring is discovered in the middle of a V-rich field and an I-rich field recently (refer to JP,8-330316,A). It is reported that this field is the I-rich field side which is not so rich as there is almost no precipitation of oxygen by being in the outside of an OSF ring when oxygen precipitation heat treatment is performed and the contrast of a deposit is checked by X-ray observation etc., and LSEPD and LFPD are formed (refer to drawing 3 (a)). And improve the temperature distribution in furnace of a pull-up machine for N field which exists only in the pole of a wafer part in the conventional CZ pull-up machine, and a pull-up rate is adjusted. F/G value (when setting a crystal pulling rate to F [mm/min] and setting the average of inclination to G [**/mm] from the melting point of silicon whenever [crystal internal temperature / of the pull-up shaft orientations between 1300 degrees C]) If it controls to the whole wafer surface and a crystal overall length by setting to 0.20-0.22mm2 / **, and min the ratio expressed with F/G, it will be proposed that it is possible to extend N field all over a wafer (refer to drawing 3 (b)).
[0008]
[Problem(s) to be Solved by the Invention] However, if it is going to extend and manufacture such a super-low defective field into the whole crystal, since this field will be limited only to N field by the side of an I-rich field, if it is an experimental aircraft, it is [with a production machine, / precision control is difficult and / a difficulty] in productivity at any rate, and is not practical [a control range is very narrow on manufacture conditions, and]. Furthermore, it became clear that it differed from the created defective distribution map (refer to drawing 1) based on the data for which this invention persons experimented and investigated the defective distribution map currently indicated by this invention, and it asked, and data sharply.
[0009] This invention was made in view of such a trouble, and its control width of face is wide, and it aims at obtaining the silicon single crystal wafer by the CZ process which is super-low defect density, maintaining the sex from Takao under the manufacture conditions which are easy to control by continuing all over the crystal with which neither a V-rich field nor an I-rich field exists.
[0010]
[Means for Solving the Problem] Invention which it was accomplished in order that this invention might attain said purpose, and was indicated to claim 1 of this invention is a silicon single crystal wafer characterized by for the nucleus of the OSF ring generated in the shape of a ring or an OSF ring existing when thermal oxidation processing is carried out, and FPD and ratio of length to diameter not existing in the whole wafer surface in the silicon single crystal wafer raised by the CZ process.
[0011] and as the manufacture approach of such a silicon single crystal wafer As indicated to claim 3 of this invention, in case a silicon single crystal is raised with the Czochrlski method When a pull-up rate is set to F [mm/min] and the average of inclination is expressed with G [**/mm] from the melting point of silicon whenever [crystal internal temperature / of the pull-up shaft orientations between 1400 degrees C], In the defective distribution map in which having set the axis of abscissa as the distance D from a crystal center to the crystal circumference [mm], and having shown defective distribution by setting an axis of ordinate as the value of F/G [mm2 / **, and min] It is the manufacture approach of the silicon single crystal wafer characterized by pulling up a crystal in the field surrounded by the boundary line of a V-rich field and N-field, and the boundary line of N-field and an I-rich field.
[0012] Thus, so that it may be settled in the field surrounded by the boundary line of a V-rich field and N-field, and the boundary line of N-field and an I-rich field based on the defective distribution map of drawing 1 which analyzed and searched for the result of an experiment and investigation If the average G of inclination is controlled from the pull-up rate F of a crystal, and the melting point of silicon whenever [crystal internal temperature / of the pull-up shaft orientations between 1400 degrees C] and a crystal is pulled up The silicon single crystal wafer with which the nucleus of the OSF ring generated in the shape of a ring or an OSF ring exists when thermal oxidation processing indicated to said claim 1 is carried out, and FPD and ratio of length to diameter do not exist in the whole wafer surface is producible.
[0013] Furthermore, it is in a concrete target. We are a crystal center about the value of said F/G, and

decided to pull up a crystal as 0.112-0.142mm2 / **, and min (claim 4).
[0014] Thus, although the field which may generate an OSF ring at the time of thermal oxidation processing has been included so that drawing 1 may see by controlling the value of F/G by the crystal center to 0.112-0.142mm2 / **, and min Since N field of OSF ring inside and outside is pulled up as the maximum expansion is carried out, a control range with inclination becomes large a pull-up rate and whenever [crystal internal temperature], manufacture conditioning becomes easy also in a production machine, and a wafer with many N fields can be produced easily.
[0015] Thus, although an OSF ring is generated in the shape of a ring or the nucleus of an OSF ring is latent when the silicon single crystal wafer obtained by the manufacture approach of this invention according to claim 3 or 4 carries out thermal oxidation processing for this wafer It is the wafer of not existing in the whole wafer surface, and all over the so-called wafer, a V-rich field and an I-rich field do not exist but FPD and ratio of length to diameter (LSEPD, LFPD) have an area of neutrality N field very big [a field], as shown in drawing 2 (b). It is the wafer which had the new defect structure which expanded N field of said OSF ring outside, and N field of the OSF ring inside to the maximum in the silicon wafer of large this invention of such an N field using N field existing also inside the OSF ring which OSF may generate in the shape of a ring when the nucleus of an OSF ring is latent and thermal oxidation processing of this wafer is carried out.
[0016] And in the silicon single crystal wafer with which invention indicated to claim 2 of this invention was raised by the CZ process, although the oxygen densities of the whole wafer surface are under 24ppma(s) (ASTM'79 value) and, as for the potential nucleus of an OSF ring, exist by oxygen precipitation heat treatment, it is the silicon single crystal wafer characterized by not generating an OSF ring when OSF thermal oxidation processing is carried out, and FPD and ratio of length to diameter not existing in the whole wafer surface. And it was made to control as the manufacture approach of such a silicon single crystal wafer, in addition to the manufacture approach indicated to claim 3 or claim 4, so that the time amount which passes through the temperature region from 1050 degrees C to 850 degrees C under said crystal becomes 140 or less minutes as indicated to claim 5 of this invention.
[0017] Thus, if the heat history is controlled as it has been 140 or less minutes about the time amount which holds down the oxygen density in a growth crystal to less than 24 ppmas, or passes through the temperature region from 1050 degrees C to 850 degrees C under growth crystal Since a device is not affected even if it can check growth of an OSF nucleus and the potential nucleus of an OSF ring or an OSF ring exists in a wafer on parenchyma, although the nucleus of an OSF ring is latent when OSF thermal oxidation processing is carried out, after all this wafer An OSF ring is not generated and they are FPD and ratio of length to diameter (it LSEPD(s)). the whole surface where neither LFPD nor an OSF ring with which the so-called whole wafer surface does damage also for a V-rich field and an I-rich field of not existing in the whole wafer surface exists -- it can continue all over an usable crystal and a wafer [defect density super-low] can be obtained. And it is possible to also make control of F/G into a large control range in this case, and a wafer can be produced easily practically.
[0018] Hereafter, although explained to a detail per this invention, this invention is not limited to these. In advance of explanation, lessons is taken from each vocabulary, and it explains beforehand.
1) K2 Cr 2O7 after cutting down a wafer from the silicon single crystal rod after growth and etching and removing a surface distortion layer with the mixed liquor of fluoric acid and a nitric acid in FPD (Flow Pattern Defect) A pit and a ripple pattern arise by etching a front face with the mixed liquor of fluoric acid and water (Secco etching). This ripple pattern is called FPD, and the defects of oxide-film pressure-proofing increase in number, so that the FPD consistency within a wafer side is high (refer to JP,4-192345,A).
[0019] 2) When the same Secco etching as FPD is performed, call SEPD (Secco Etch Pit Defect) a thing without FPD, a call, and a flow pattern for the thing accompanied by a flow pattern (flow pattern) with SEPD. When it is thought in this that large SEPD (LSEPD) 10 micrometers or more originates in a rearrangement cluster and a rearrangement cluster exists in a device, a current leaks through this rearrangement and it stops achieving the function as a P-N junction.
[0020] 3) Cut down a wafer from the silicon single crystal rod after growth, and carry out cleavage of the wafer to LSTD (Laser Scattering Tomography Defect) after etching and removing a surface

distortion layer with the mixed liquor of fluoric acid and a nitric acid. Incidence of the infrared light can be carried out from this cleavage plane, and the defect scattering light which exists in a wafer can be detected by detecting the light which came out from the wafer front face. About the scatterer observed here, it is a society etc., there is already a report, and it is regarded as the oxygen sludge (J. J.A.P. Vol.32, P3679, 1993 reference). Moreover, the result that it is the void (hole) of octahedron is also reported by the latest research.

[0021] 4) the defect which becomes the cause of degrading oxide film pressure-proofing of the core of a wafer, with COP (Crystal Originated Particle) -- it is -- Secco -- by SC-1 washing (washing by the mixed liquor of NH4 OH:H2 O2:H2 O=1:1:10), the defect set to FPD if dirty works as a selection etching reagent, and is set to COP. The diameter of this pit is investigated with light scattering measurement by 1 micrometer or less.

[0022] 5) It is the defect which there are LSEPD, LFPD, etc. in ratio of length to diameter (Large Dislocation: cable address of the dislocation loop between grids), and is considered to be a dislocation loop reason. A large thing 10 micrometers or more is said that LSEPD described above also in SEPD. Moreover, also in FPD which LFPD described above, the magnitude of a tip pit says a large thing 10 micrometers or more, and it is considered the dislocation loop reason also here.

[0023] the place investigated in the detail about the boundary neighborhood of V field and an I region about the silicon single crystal growth by the CZ process as this invention persons proposed by Japanese Patent Application No. No. 199415 [nine to] previously -- **** of this boundary neighborhood -- the narrow field had few FPD(s), LSTD(s), and COP remarkably, and it discovered that there was a neutral field where LSEPD does not exist, either.

[0024] Then, if this neutral field can be extended all over a wafer, it will conceive that a point defect can be reduced sharply, and since the pull-up rate is almost fixed in the wafer side of a crystal, the main factors which determine concentration distribution of the point defect within a field will be temperature gradients in a growth (pull-up) rate and the relation of a temperature gradient. That a difference is in the temperature gradient of shaft orientations in a wafer side that is, on a problem If this difference can be reduced, that the concentration difference of the point defect within a wafer side can also be reduced A header, When controlling whenever [furnace temperature], pulling up the difference of the temperature gradient Gc of the crystal center section, and the temperature gradient germanium of a crystal circumference part so that it might be set to **G=(germanium-Gc) <=5 degree-C/cm, and adjusting the rate, a wafer without the defect which the whole wafer surface becomes from N field came to be obtained.

[0025] In this invention, as a result of difference **G of the above temperature gradients using the crystal pulling equipment by the small CZ process, changing a pull-up rate and investigating the inside of the crystal face, the following knowledge was newly acquired. Although N field which exists between a V-rich field and an I-rich field was conventionally considered to be only the outside of an OSF ring (nucleus), it checked that N field existed also inside an OSF ring (refer to drawing 2 (a)). namely, the case of above-mentioned Japanese Patent Application No. No. 199415 [nine to] -- an OSF ring -- a V-rich field and the border area of N field -- becoming -- **** (refer to drawing 3 (a)) -- it turned out that these two are not necessarily in agreement. This is not discovered when it experiments with the large crystal pulling equipment of the conventional **G, but as a result of investigating the crystal which used the small crystal pulling equipment of the **G above-mentioned this time, it is discovered.

[0026] Whenever [furnace temperature / of the pull-up equipment in this investigation] was wholeheartedly analyzed using the comprehensive heat transfer analysis software FEMAG (F. 33 Dupret, P.Nicodeme, Y.Ryckmans, P.Wouters, and M.J.Crochet, Int.J.Heat MassTransfer, 1849 (1990)).

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to a silicon single crystal wafer with few crystal defects, and its manufacture approach.
[0002]
[Description of the Prior Art] In recent years, the quality demand to the silicon single crystal produced with the Czochrlski method (it is hereafter written as a CZ process) used as the substrate has been increasing with detailed-izing of the component accompanying high integration of a semiconductor circuit. The defect of a single crystal growth reason in which the oxide film proof-pressure property especially called grown-in (Grown-in) defects, such as FPD, LSTD, and COP, and the property of a device are worsened exists, and importance is attached to reduction of the consistency and size.
[0003] In explaining these defects, it explains being known generally about the factor which determines each concentration of the point defect of the hole mold first called the Vacancy (it may outline Vacancy and Following V) incorporated by the silicon single crystal, and the mold silicon point defect between grids called Interstitial-Si (it may outline Interstitial-Si and Following I) incorporated.
[0004] In a silicon single crystal, V fields are Vacancy, i.e., the crevice generated from lack of a silicon atom, and a field with many things like a hole. With an I region It is the thing of a field with many lumps of the rearrangement and the excessive silicon atom which are generated when a silicon atom exists too much. Between V field and an I region The neutral (it may outline Neutral and Following N) field without lack of an atom or an excess (few) will exist. And with [even if said grown-in defects (FPD, LSTD, COP, etc.) occur when V and I are in a condition / ****** / to the last, and it has the bias of some atoms] saturation [below], it has turned out that it does not exist as a defect.
[0005] The concentration of both this point defect is decided from the pull-up rate (growth rate) of the crystal in a CZ process, and relation with the temperature gradient G near [under crystal] the solid-liquid interface, and existence of the defect of the shape of a ring called OSF (an oxidation induction stacking fault, Oxidation Indused Stacking Fault) is checked in the boundary neighborhood of V field and an I region.
[0006] A classification of the defect of these crystal growth reason calls the V-rich field the field where grown-in defects by which it is considered as the void reason to which hole type point defects gathered when a growth rate is a high speed comparatively, the above before and after 0.6 mm/min and, such as FPD, LSTD, and COP, exist in high density throughout the direction of the diameter of a crystal, and these defects exist (refer to drawing 4 (a)). Moreover, when a growth rate is 0.6 or less mm/min, the field where the above-mentioned OSF ring is generated from the circumference of a crystal with the fall of a growth rate, the defect of ratios of length to diameter (Large Dislocation: the cable address of the dislocation loop between grids, LSEPD, LFPD, etc.) considered to be dislocation loop reasons by the outside of this ring exists in a low consistency, and these defects exist is called the I-rich field (refer to drawing 4 (b)). Furthermore, if a growth rate is made into a low speed 0.4 mm/min order, an OSF ring will condense and disappear at the core of a wafer, and the whole surface will serve as an I-rich field (drawing 4 (c)).

[0007] Moreover, the existence of the field where neither FPD of a hole reason, LSTD, COP nor LSEPD of a dislocation loop reason and LFPD exist called N field to the outside of an OSF ring is discovered in the middle of a V-rich field and an I-rich field recently (refer to JP,8-330316,A). It is reported that this field is the I-rich field side which is not so rich as there is almost no precipitation of oxygen by being in the outside of an OSF ring when oxygen precipitation heat treatment is performed and the contrast of a deposit is checked by X-ray observation etc., and LSEPD and LFPD are formed (refer to drawing 3 (a)). And improve the temperature distribution in furnace of a pull-up machine for N field which exists only in the pole of a wafer part in the conventional CZ pull-up machine, and a pull-up rate is adjusted. F/G value (when setting a crystal pulling rate to F [mm/min] and setting the average of inclination to G [**/mm] from the melting point of silicon whenever [crystal internal temperature / of the pull-up shaft orientations between 1300 degrees C]) If it controls to the whole wafer surface and a crystal overall length by setting to 0.20-0.22mm2 / **, and min the ratio expressed with F/G, it will be proposed that it is possible to extend N field all over a wafer (refer to drawing 3 (b)).

[0008]

[Problem(s) to be Solved by the Invention] However, if it is going to extend and manufacture such a super-low defective field into the whole crystal, since this field will be limited only to N field by the side of an I-rich field, if it is an experimental aircraft, it is [with a production machine, / precision control is difficult and / a difficulty] in productivity at any rate, and is not practical [a control range is very narrow on manufacture conditions, and]. Furthermore, it became clear that it differed from the created defective distribution map (refer to drawing 1) based on the data for which this invention persons experimented and investigated the defective distribution map currently indicated by this invention, and it asked, and data sharply.

[0009] This invention was made in view of such a trouble, and its control width of face is wide, and it aims at obtaining the silicon single crystal wafer by the CZ process which is super-low defect density, maintaining the sex from Takao under the manufacture conditions which are easy to control by continuing all over the crystal with which neither a V-rich field nor an I-rich field exists.

[0010]

[Means for Solving the Problem] Invention which it was accomplished in order that this invention might attain said purpose, and was indicated to claim 1 of this invention is a silicon single crystal wafer characterized by for the nucleus of the OSF ring generated in the shape of a ring or an OSF ring existing when thermal oxidation processing is carried out, and FPD and ratio of length to diameter not existing in the whole wafer surface in the silicon single crystal wafer raised by the CZ process.

[0011] and as the manufacture approach of such a silicon single crystal wafer As indicated to claim 3 of this invention, in case a silicon single crystal is raised with the Czochrlski method When a pull-up rate is set to F [mm/min] and the average of inclination is expressed with G [**/mm] from the melting point of silicon whenever [crystal internal temperature / of the pull-up shaft orientations between 1400 degrees C], In the defective distribution map in which having set the axis of abscissa as the distance D from a crystal center to the crystal circumference [mm], and having shown defective distribution by setting an axis of ordinate as the value of F/G [mm2 / **, and min] It is the manufacture approach of the silicon single crystal wafer characterized by pulling up a crystal in the field surrounded by the boundary line of a V-rich field and N-field, and the boundary line of N-field and an I-rich field.

[0012] Thus, so that it may be settled in the field surrounded by the boundary line of a V-rich field and N-field, and the boundary line of N-field and an I-rich field based on the defective distribution map of drawing 1 which analyzed and searched for the result of an experiment and investigation If the average G of inclination is controlled from the pull-up rate F of a crystal, and the melting point of silicon whenever [crystal internal temperature / of the pull-up shaft orientations between 1400 degrees C] and a crystal is pulled up The silicon single crystal wafer with which the nucleus of the OSF ring generated in the shape of a ring or an OSF ring exists when thermal oxidation processing indicated to said claim 1 is carried out, and FPD and ratio of length to diameter do not exist in the whole wafer surface is producible.

[0013] Furthermore, it is in a concrete target. We are a crystal center about the value of said F/G, and

decided to pull up a crystal as 0.112-0.142mm2 / **, and min (claim 4).
[0014] Thus, although the field which may generate an OSF ring at the time of thermal oxidation processing has been included so that drawing 1 may see by controlling the value of F/G by the crystal center to 0.112-0.142mm2 / **, and min Since N field of OSF ring inside and outside is pulled up as the maximum expansion is carried out, a control range with inclination becomes large a pull-up rate and whenever [crystal internal temperature], manufacture conditioning becomes easy also in a production machine, and a wafer with many N fields can be produced easily.
[0015] Thus, although an OSF ring is generated in the shape of a ring or the nucleus of an OSF ring is latent when the silicon single crystal wafer obtained by the manufacture approach of this invention according to claim 3 or 4 carries out thermal oxidation processing for this wafer It is the wafer of not existing in the whole wafer surface, and all over the so-called wafer, a V-rich field and an I-rich field do not exist but FPD and ratio of length to diameter (LSEPD, LFPD) have an area of neutrality N field very big [a field], as shown in drawing 2 (b). It is the wafer which had the new defect structure which expanded N field of said OSF ring outside, and N field of the OSF ring inside to the maximum in the silicon wafer of large this invention of such an N field using N field existing also inside the OSF ring which OSF may generate in the shape of a ring when the nucleus of an OSF ring is latent and thermal oxidation processing of this wafer is carried out.
[0016] And in the silicon single crystal wafer with which invention indicated to claim 2 of this invention was raised by the CZ process, although the oxygen densities of the whole wafer surface are under 24ppma(s) (ASTM'79 value) and, as for the potential nucleus of an OSF ring, exist by oxygen precipitation heat treatment, it is the silicon single crystal wafer characterized by not generating an OSF ring when OSF thermal oxidation processing is carried out, and FPD and ratio of length to diameter not existing in the whole wafer surface. And it was made to control as the manufacture approach of such a silicon single crystal wafer, in addition to the manufacture approach indicated to claim 3 or claim 4, so that the time amount which passes through the temperature region from 1050 degrees C to 850 degrees C under said crystal becomes 140 or less minutes as indicated to claim 5 of this invention.
[0017] Thus, if the heat history is controlled as it has been 140 or less minutes about the time amount which holds down the oxygen density in a growth crystal to less than 24 ppmas, or passes through the temperature region from 1050 degrees C to 850 degrees C under growth crystal Since a device is not affected even if it can check growth of an OSF nucleus and the potential nucleus of an OSF ring or an OSF ring exists in a wafer on parenchyma, although the nucleus of an OSF ring is latent when OSF thermal oxidation processing is carried out, after all this wafer An OSF ring is not generated and they are FPD and ratio of length to diameter (it LSEPD(s)). the whole surface where neither LFPD nor an OSF ring with which the so-called whole wafer surface does damage also for a V-rich field and an I-rich field of not existing in the whole wafer surface exists -- it can continue all over an usable crystal and a wafer [defect density super-low] can be obtained. And it is possible to also make control of F/G into a large control range in this case, and a wafer can be produced easily practically.
[0018] Hereafter, although explained to a detail per this invention, this invention is not limited to these. In advance of explanation, lessons is taken from each vocabulary, and it explains beforehand.
1) K2 Cr 2O7 after cutting down a wafer from the silicon single crystal rod after growth and etching and removing a surface distortion layer with the mixed liquor of fluoric acid and a nitric acid in FPD (Flow Pattern Defect) A pit and a ripple pattern arise by etching a front face with the mixed liquor of fluoric acid and water (Secco etching). This ripple pattern is called FPD, and the defects of oxide-film pressure-proofing increase in number, so that the FPD consistency within a wafer side is high (refer to JP,4-192345,A).
[0019] 2) When the same Secco etching as FPD is performed, call SEPD (Secco Etch Pit Defect) a thing without FPD, a call, and a flow pattern for the thing accompanied by a flow pattern (flow pattern) with SEPD. When it is thought in this that large SEPD (LSEPD) 10 micrometers or more originates in a rearrangement cluster and a rearrangement cluster exists in a device, a current leaks through this rearrangement and it stops achieving the function as a P-N junction.
[0020] 3) Cut down a wafer from the silicon single crystal rod after growth, and carry out cleavage of the wafer to LSTD (Laser Scattering Tomography Defect) after etching and removing a surface

distortion layer with the mixed liquor of fluoric acid and a nitric acid. Incidence of the infrared light can be carried out from this cleavage plane, and the defect scattering light which exists in a wafer can be detected by detecting the light which came out from the wafer front face. About the scatterer observed here, it is a society etc., there is already a report, and it is regarded as the oxygen sludge (J. J.A.P. Vol.32, P3679, 1993 reference). Moreover, the result that it is the void (hole) of octahedron is also reported by the latest research.

[0021] 4) the defect which becomes the cause of degrading oxide film pressure-proofing of the core of a wafer, with COP (Crystal Originated Particle) -- it is -- Secco -- by SC-1 washing (washing by the mixed liquor of NH4 OH:H2 O2:H2 O=1:1:10), the defect set to FPD if dirty works as a selection etching reagent, and is set to COP. The diameter of this pit is investigated with light scattering measurement by 1 micrometer or less.

[0022] 5) It is the defect which there are LSEPD, LFPD, etc. in ratio of length to diameter (Large Dislocation: cable address of the dislocation loop between grids), and is considered to be a dislocation loop reason. A large thing 10 micrometers or more is said that LSEPD described above also in SEPD. Moreover, also in FPD which LFPD described above, the magnitude of a tip pit says a large thing 10 micrometers or more, and it is considered the dislocation loop reason also here.

[0023] the place investigated in the detail about the boundary neighborhood of V field and an I region about the silicon single crystal growth by the CZ process as this invention persons proposed by Japanese Patent Application No. No. 199415 [nine to] previously -- **** of this boundary neighborhood -- the narrow field had few FPD(s), LSTD(s), and COP remarkably, and it discovered that there was a neutral field where LSEPD does not exist, either.

[0024] Then, if this neutral field can be extended all over a wafer, it will conceive that a point defect can be reduced sharply, and since the pull-up rate is almost fixed in the wafer side of a crystal, the main factors which determine concentration distribution of the point defect within a field will be temperature gradients in a growth (pull-up) rate and the relation of a temperature gradient. That a difference is in the temperature gradient of shaft orientations in a wafer side that is, on a problem If this difference can be reduced, that the concentration difference of the point defect within a wafer side can also be reduced A header, When controlling whenever [furnace temperature], pulling up the difference of the temperature gradient Gc of the crystal center section, and the temperature gradient germanium of a crystal circumference part so that it might be set to **G=(germanium-Gc) <=5 degree-C/cm, and adjusting the rate, a wafer without the defect which the whole wafer surface becomes from N field came to be obtained.

[0025] In this invention, as a result of difference **G of the above temperature gradients using the crystal pulling equipment by the small CZ process, changing a pull-up rate and investigating the inside of the crystal face, the following knowledge was newly acquired. Although N field which exists between a V-rich field and an I-rich field was conventionally considered to be only the outside of an OSF ring (nucleus), it checked that N field existed also inside an OSF ring (refer to drawing 2 (a)). namely, the case of above-mentioned Japanese Patent Application No. No. 199415 [nine to] -- an OSF ring -- a V-rich field and the border area of N field -- becoming -- **** (refer to drawing 3 (a)) -- it turned out that these two are not necessarily in agreement. This is not discovered when it experiments with the large crystal pulling equipment of the conventional **G, but as a result of investigating the crystal which used the small crystal pulling equipment of the **G above-mentioned this time, it is discovered.

[0026] Whenever [furnace temperature / of the pull-up equipment in this investigation] was wholeheartedly analyzed using the comprehensive heat transfer analysis software FEMAG (F. 33 Dupret, P.Nicodeme, Y.Ryckmans, P.Wouters, and M.J.Crochet, Int.J.Heat MassTransfer, 1849 (1990)). When a pull-up rate is set to F [mm/min] and the average of inclination is expressed with G [**/mm] from the melting point of silicon whenever [crystal internal temperature / of the pull-up shaft orientations between 1400 degrees C], the value of F/G consequently, in a crystal center If it pulls up and a rate F and the temperature gradient average G are controlled to become within the limits of 0.112-0.142mm2 / **, and min Although the nucleus of the OSF ring generated in the shape of a ring or an OSF ring existed when OSF thermal oxidation processing was carried out, it turned out that the silicon single crystal wafer with which FPD and ratio of length to diameter do not exist in the whole wafer surface is obtained.

[0027] Although drawing 1 is the case where a silicon single crystal with a diameter of 6 inches is made into an example, it expresses many defective distribution at the time of setting an axis of abscissa as the direction location of a path of a crystal, and setting an axis of ordinate as F/G value. Between a crystal center location and the location from a core to about 50mm, the boundary of a V-rich field / N field goes up gently from 0.142mm2 / **, and min, and if it applies to a periphery from this location, it is on the line which increased F/G value rapidly, so that clearly from drawing 1 . The cores of an OSF ring field are about 0.125mm2 / **, and min, and if it applies to a crystal periphery, they are on the line which increased F/G value rapidly almost in parallel with the boundary line of a V-rich field / N field. Furthermore, the boundary with N field / I-rich field was set to 0.112mm2 / **, and min between the crystal center location and the location from a core to about 70mm, and has fallen rapidly toward the crystal periphery after that. Therefore, what is necessary is just to make it become 0.112-0.142mm2 / **, and min in a crystal center location, in order to make the most of N field in the wafer containing an OSF ring.
[0028] When this was explained in respect of the wafer, as it was conventionally shown in drawing 3 (a) Although N field which exists in the outside of the OSF ring in a usual pull-up rate and crystal pulling equipment tended to be pulled up using special crystal pulling equipment that it should expand all over a crystal (refer to drawing 3 (b)), a rate and **G tended to be controlled and it was going to manufacture the defect-free crystal Control was difficult, and the control width of face of manufacture conditions, such as a pull-up rate and a temperature gradient, is very narrow, and it was not [the difficulty was in productivity and] practical.
[0029] In this invention, it did not limit only to N field of the outside of an OSF ring, but N field was made to carry out the maximum expansion also using N field (refer to drawing 2 (a)) which exists also inside the OSF ring discovered this time. That is, the pull-up rate, **G, and crystal pulling equipment to which N field can be expanded all over the maximum wafer while the OSF ring had been included, as shown in drawing 2 (b) were chosen and pulled up. Consequently, if it pulls up so that it may fall within the range of F/G value which was described above, and inclination is adjusted and pulled up a rate and whenever [crystal internal temperature], the wafer of a low defect can be easily manufactured under manufacture conditions with the control width of face expanded conventionally.
[0030] It turns out that an OSF ring is not generated by thermal oxidation processing even if the nucleus of an OSF ring exists in the whole wafer surface from the latest research in the case of hypoxia concentration, and a device is not affected about an OSF ring on the other hand. If the oxygen density in the whole wafer surface is less than 24 ppmas as a result of using the same crystal pulling equipment for the threshold value of this oxygen density and pulling up the crystal of some kinds of oxygen density level, when thermal oxidation processing of a wafer is performed, it is checked that an OSF ring is not generated.
[0031] That is, although it is to 24ppma(s) that the nucleus which serves as OSF covering a crystal overall length exists when drawing 5 pulls up the crystal of one and an oxygen density is gradually lowered to inside, but an OSF ring is observed when thermal oxidation processing of a wafer is performed and an OSF ring nucleus exists in less than 24 ppmas, it means that the OSF ring by thermal oxidation processing is not generated.
[0032] Incidentally, in order to set the oxygen density under growth crystal to less than 24 ppmas, that what is necessary is just to carry out by the approach generally used from the former, distribution etc. can be adjusted whenever [rotational frequency / of a crucible /, or melt internal temperature], and the means of controlling the convection current of melt can perform easily.
[0033] In addition, even if an OSF ring is not generated, there is an inclination for precipitation of oxygen to decrease, in the place where the nucleus exists, but since strong gettering is not required in the bottom process of low temperature of a device, either, the little of the precipitation of oxygen in an OSF field does not become a problem.
[0034] Subsequently, the conditions which check growth of an OSF ring nucleus were examined. So that some kinds of crystal pulling equipments (what changed the configuration in a furnace) with which temperature distribution in furnace differs may be used and an OSF ring may be generated at the time of OSF thermal oxidation processing Into the crystal which gave the heat history which passes through a 1050-850-degree C temperature zone region in 140 or less minutes as a result of

controlling a pull-up rate and pulling up a crystal OSF thermal oxidation processing in which the existence of OSF ring generating is checked after that is performed. The ** OSF ring was not checked (I.). [Yamashita] and Y.Shimanuki:The Electrochemical SocietyExtended Abstract and Los Angels, Carifornia, and May7- 12, 1989, and P.346 reference.
[0035] Then, in addition to F / G value control, an oxygen density is held down to less than 24 ppmas during a crystal. Or if the heat history which passes through the temperature region from 1050 degrees C to 850 degrees C of a growth crystal is controlled as it has been 140 or less minutes, and growth of an OSF ring nucleus is checked When OSF thermal oxidation processing is carried out, there is nothing, FPD and ratio of length to diameter do not exist, but the whole crystal surface is occupied in an usable field, and generating of an OSF ring can produce a defect-free crystal in the large condition range.
[0036] Namely, in case a silicon single crystal is raised by the CZ process, a pull-up rate is set to F [mm/min]. When the average of inclination is expressed with G [**/mm] from the melting point of silicon whenever [crystal internal temperature / of the pull-up shaft orientations between 1400 degrees C], the value of F/G in a crystal center Control to 0.112-0.142mm2 / **, and min, and an oxygen density is held down to less than 24 ppmas during a crystal. Or by controlling so that the time amount which passes through the temperature region from 1050 degrees C to 850 degrees C under said crystal becomes 140 or less minutes the whole surface which an OSF ring does not generate even if it carries out thermal oxidation processing, while having large N field -- an usable defect-free wafer can be easily manufactured under the conditions that control width of face is wide.
[0037]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained to a detail, referring to a drawing. First, drawing 6 R> 6 explains the example of a configuration of the crystal pulling equipment by the CZ process used by this invention. As shown in drawing 6 , this crystal pulling equipment 30 The pull-up room 31, the crucible 32 prepared all over the pull-up room 31, and the heater 34 arranged around a crucible 32, It has the reel style (not shown) which rotates or rolls round the crucible maintenance shaft 33 made to rotate a crucible 32 and its rolling mechanism (not shown), the seed chuck 6 holding the seed crystal 5 of silicon, the cable 7 that pulls up a seed chuck 6, and a cable 7, and is constituted. A quartz crucible is prepared in the side in which a crucible 32 holds the silicon melt (molten bath) 2 of the inside, and the graphite crucible is prepared in the outside. Moreover, the heat insulator 35 is arranged around [outside] the heater 34.
[0038] Moreover, in order to set up the manufacture conditions in connection with the manufacture approach of this invention, the annular solid-liquid interface heat insulator 8 is formed in the periphery of the solid-liquid interface of a crystal, and the up surrounding heat insulator 9 is arranged on it. This solid-liquid interface heat insulator 8 forms the 3-5cm clearance 10 between that lower limit and surface of hot water of silicon melt 2, and is installed in it. The up surrounding heat insulator 9 may not be used depending on conditions. Furthermore, coolant gas is sprayed or the tubed cooling system 36 which interrupts radiant heat and cools a single crystal is formed. Independently, by installing the magnet which is not illustrated in the horizontal outside of the pull-up room 31, and impressing magnetic fields, such as a horizontal direction or a perpendicular direction, to silicon melt 2, the convection current of melt is controlled and, recently, the so-called MCZ method for measuring the stable growth of a single crystal is used in many cases.
[0039] Next, the single-crystal-growth approach by above crystal pulling equipment 30 is explained. First, within a crucible 32, the high grade polycrystal raw material of silicon is heated more than the melting point (about 1420-degreeC), and is dissolved. Next, the tip of a seed crystal 5 is made contacted or immersed in the surface abbreviation core of melt 2 by beginning to roll a cable 7. Then, while rotating the crucible maintenance shaft 33 in the proper direction, single crystal growth is started by rolling round rotating a cable 7 and pulling up a seed crystal 5. Henceforth, the single crystal rod 1 of an approximate circle column configuration can be obtained by adjusting a pull-up rate and temperature appropriately.
[0040] In this case, in this invention, especially in order to attain the purpose of this invention, as shown in drawing 6 , in the periphery space of the liquefied part in the single crystal rod 1 on the surface of hot water of the pull-up room 31, it is important that the temperature of the crystal near the surface of hot water formed the annular solid-liquid interface heat insulator 8 in the temperature

region from 1420 degrees C to 1400 degrees C and to have arranged the up surrounding heat insulator 9 on it. Furthermore, it is good also as structure which should form the equipment 36 which cools a crystal, for example, a cooling system, in the upper part of this heat insulator if needed, should spray coolant gas on this from the upper part, should cool the crystal, and attached the radiant heat reflecting plate in the cylinder lower part.

[0041] Thus, since a heat insulation effect is acquired by radiant heat near the crystal growth interface and the radiant heat from a heater etc. can be cut in the upper part of a crystal by establishing a predetermined clearance in the location of the right above of an oil level, arranging a heat insulator, and considering as the structure which formed further the equipment which cools a crystal in the upper part of this heat insulator, the manufacture conditions of this invention can be satisfied. An air-cooling duct, a water-cooled coil, etc. which surround the perimeter of a crystal are formed, and you may make it secure a desired temperature gradient independently [said tubed cooling system 36] as a cooling system of this crystal.

[0042] Conventional equipment was shown in drawing 7 for the crystal pulling equipment used by this invention, and a comparison. Although it is the same as the pull-up equipment used by this invention about fundamental structure, neither the solid-liquid interface heat insulator 8, the up surrounding heat insulator 9 nor the cooling system 36 is equipped.

[0043]

[Example] Although an example is given and the gestalt of concrete operation of this invention is explained hereafter, this invention is not limited to these.

(Example 1) It raised, having charged 60kg of raw material polycrystalline silicon to the 20 inch quartz crucible, and lowering an average pull-up rate for the diameter of 6 inches, and the silicon single crystal rod of bearing <100> to 0.88 - 0.50 mm/min with the pull-up equipment 30 shown in drawing 6 , (body die length of about 85cm of a single crystal rod). It was made into 4cm space from about 1420 degrees C and the surface of hot water up to the lower limit of an annular solid-liquid interface heat insulator, on it, the water temperature of silicon melt has arranged the annular solid-liquid interface heat insulator of 10cm height, it adjusted the crucible maintenance shaft, set the height from the surface of hot water to pull-up room head lining as 30cm, and arranged the up surrounding heat insulator. And F/G value in the crystal center section were changed to 0.22-0.10mm2 and **/min, and was pulled up.

[0044] From the single crystal rod obtained here, the wafer was cut down, mirror plane processing was performed, the mirror plane wafer of a silicon single crystal was produced, and the grown-in defect was measured. Moreover, thermal oxidation processing was performed and the existence of OSF ring generating was checked. Consequently, although the OSF ring field which F/G value generates from the wafer periphery section in about 15mm location at the time of thermal oxidation processing within the limits of 0.112-0.142mm2 / **, and min existed, the super-low defective wafer which carried out the maximum expansion of the N field where the grown-in defect of these ring inside and outside does not exist was obtained. In addition, the oxide-film proof-pressure property of this wafer became 100% of rates of C-mode excellent article. In addition, the C-mode Measuring condition is as follows.

1) Oxide-film thickness : 25nm Two measuring electrode: Phosphorus dope polish recon 3 electrode-surface product: 8mm2 4 judging current: 1 mA/cm2 5 excellent-article judging: Dielectric-breakdown electric field judged the thing of 8 or more MV/cm to be an excellent article.

[0045] (Example 2) Except having carried out by lowering an oxygen density gradually during crystal pulling, it pulled up on the same conditions as an example 1, and from the obtained single crystal rod, the wafer was cut down, mirror plane processing was performed, the mirror plane wafer of a silicon single crystal was produced, and the grown-in defect was measured. Moreover, thermal oxidation processing was performed and the existence of OSF ring generating was checked.

[0046] Consequently, F/G value of the wafer of 24 or more ppmas was the super-low defective wafers with which the oxygen density within a wafer side has an OSF ring from a wafer core in N field in which a whole surface grown-in defect does not exist in about 15mm location within the limits of 0.112-0.142mm2 / **, and min. On the other hand, the oxygen density within a wafer side was the defect-free wafer which does not generate an OSF ring by thermal oxidation processing, although the OSF nucleus existed in N field in which, as for the wafer of less than 24 ppmas, a whole

surface grown-in defect does not exist. In addition, the oxide-film proof-pressure property of this wafer became 100% of rates of C-mode excellent article.
[0047] (Example 3) Except having given the heat history which made time amount which passes through the temperature region to 1050-850 degrees C under crystal 140 or less minutes during crystal pulling, it pulled up on the same conditions as an example 1, and from the obtained single crystal rod, the wafer was cut down, mirror plane processing was performed, the mirror plane wafer of a silicon single crystal was produced, and the grown-in defect was measured. Moreover, thermal oxidation processing was performed and the existence of OSF ring generating was checked.
[0048] Consequently, even if the oxygen density was the thing of 27ppma(s), F/G value was the defect-free wafers which do not generate an OSF ring by thermal oxidation processing, although the OSF nucleus existed in N field in which a whole surface grown-in defect does not exist within the limits of 0.112-0.142mm2 / **, and min. In addition, the oxide-film proof-pressure property of this wafer became 100% of rates of C-mode excellent article.
[0049] In addition, this invention is not limited to the above-mentioned operation gestalt. The above-mentioned operation gestalt is instantiation, and no matter it may be what thing which has the same configuration substantially with the technical thought indicated by the claim of this invention, and does the same operation effectiveness so, it is included by the technical range of this invention.
[0050] For example, although the example was given and explained per in the above-mentioned operation gestalt when a silicon single crystal with a diameter of 6 inches was raised When this invention is not limited to this, but a pull-up rate is set to F [mm/min] and the average of inclination is expressed with G [**/mm] from the melting point of silicon whenever [crystal internal temperature / of the pull-up shaft orientations between 1400 degrees C], the value of F/G in a crystal center If it controls to be set to 0.112-0.142mm2 / **, and min, it is applicable also to the diameter of 8-16 inches, or the silicon single crystal beyond it. Moreover, it cannot be overemphasized that this invention is applicable also to the so-called MCZ method for impressing a level magnetic field and length magnetic field, a cusp field, etc. to silicon melt.
[0051] Furthermore, in the above-mentioned operation gestalt, although hypoxia-izing and heat history control were explained separately, both both may be carried out and an OSF ring can be defanged more certainly.
[0052]
[Effect of the Invention] As explained above, according to this invention, the control width of face of single-crystal-growth conditions becomes large, and the wafer to which the maximum N field was expanded can be easily produced by using N field of an OSF ring outside, an OSF ring or an OSF nucleus, and N field of the inside. And if hypoxia-izing or control of the heat history of a low-temperature region is used together, an OSF ring will not be generated, either, but a glow in defect can also manufacture a silicon single crystal wafer with the defect-free whole wafer surface of super-low level.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] They are many defective distribution maps at the time of setting an axis of abscissa as the direction location of a path of the crystal within a silicon single crystal wafer side, and setting an axis of ordinate as F/G value.
[Drawing 2] It is an explanatory view showing the many [within the crystal face] defective distribution discovered by this invention.
(a) When it pulls up on the usual pull-up conditions and pulls up on the pull-up conditions of (b) this invention.
[Drawing 3] It is an explanatory view showing the many [within the crystal face] defective distribution in an approach to pull up the former.
(a) When it pulls up on the usual pull-up conditions, and precision control was carried out and inclination is pulled up (b) pull-up rate and whenever [crystal internal temperature].
[Drawing 4] It is an explanatory view showing the relation between the pull-up rate in an approach to pull up the former, and the defective distribution within the crystal face.
(a) In a high-speed pull-up, in (b) medium-speed pull-up, it is in (c) low-speed pull-up.
[Drawing 5] In this invention, the boundary location of the generating field of the OSF ring at the time of performing thermal oxidation processing to a wafer and the existence region of an OSF nucleus is an explanatory view showing being influenced by the oxygen density during a crystal.
(a) In the graph and (b) crystal longitudinal section showing the die-length direction location of a crystal rod, and the relation of an oxygen density, it is the explanatory view showing the boundary location of the generating field of an OSF ring, and the existence region of an OSF nucleus.
[Drawing 6] It is the approximate account Fig. of the crystal pulling equipment by the CZ process used by this invention.
[Drawing 7] It is the approximate account Fig. of the conventional crystal pulling equipment by the CZ process.
[Description of Notations]
1 -- Growth single crystal rod,
2 -- Silicon melt,
3 -- Surface of hot water,
4 -- Solid-liquid interface,
5 -- Seed crystal,
6 -- Seed chuck,
7 -- Cable,
8 -- Solid-liquid interface heat insulator,
9 -- Up surrounding heat insulator,
10 -- Clearance between the surface of hot water and a solid-liquid interface heat insulator lower limit,
30 -- Crystal pulling equipment,
31 -- Pull-up room,
32 -- Crucible,
33 -- Crucible maintenance shaft,
34 -- Heater,

35 -- Heat insulator,
36 -- Cooling system.
V -- V-rich field,
N --N - field,
I -- I-rich field,
OR -- OSF ring.

[Translation done.]

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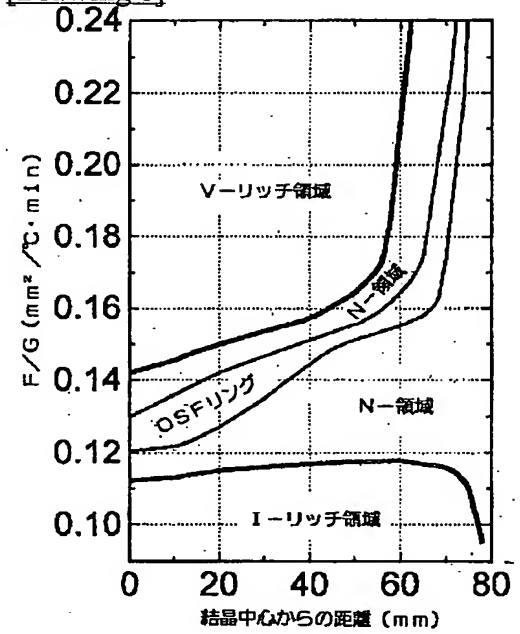
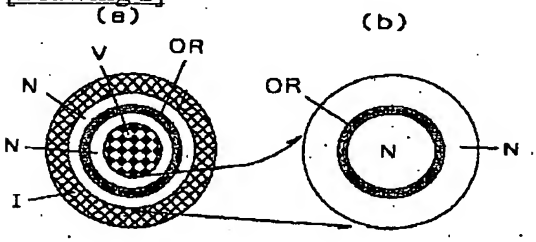
DRAWINGS

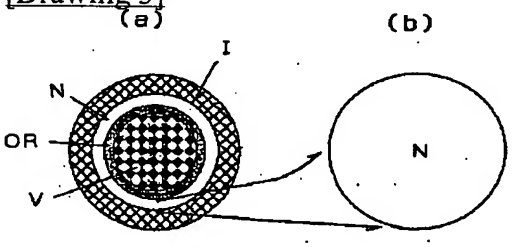
[Drawing 1]



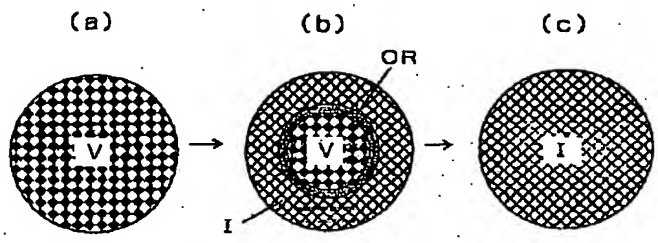
[Drawing 2]



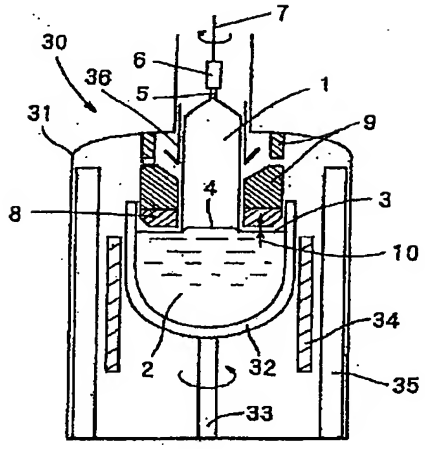
[Drawing 3]



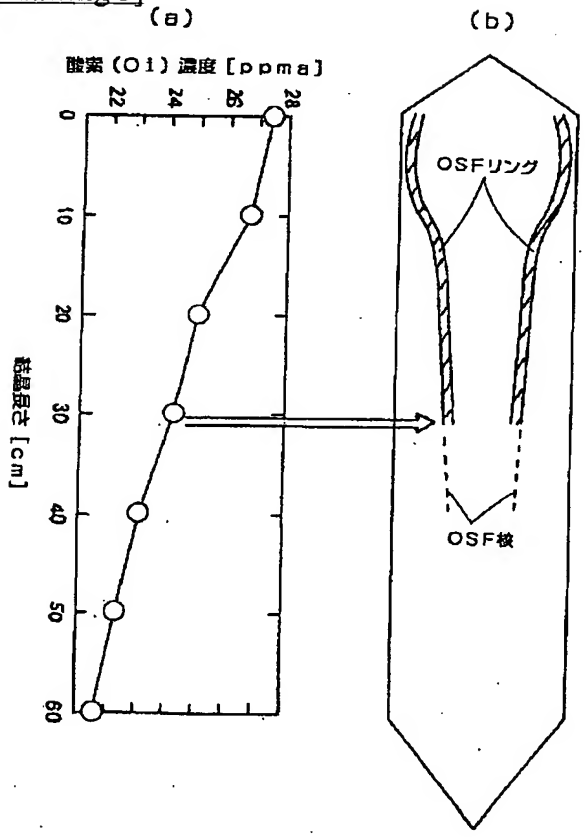
[Drawing 4]



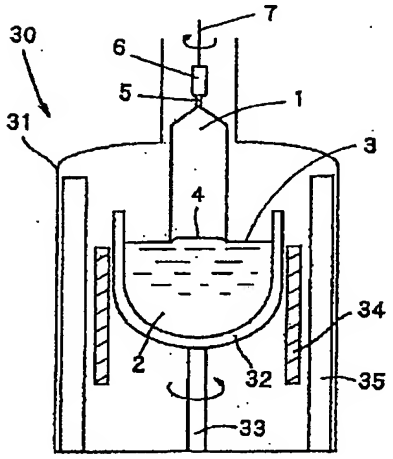
[Drawing 6]



[Drawing 5]



[Drawing 7]



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